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| EXAMINER | |
|---|---|
| HENRY, MATTHEW ALLAN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2116 | |

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/017,125 | MARES, MIRCEA | |
| | Examiner | Art Unit | |
| | Matthew A. Henry | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/17,3/14,7/18/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Protected and Redundant Electric Load Management Center.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "sense resistor" in Line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. There is no reference in either Claim 1, upon which Claim 4 is dependent, or Claim 4 itself of a sense resistor being included in the claimed electrical power distribution center.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**2. Claims 1 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darty (5,752,047) in view of Maher (5,723,915), Smith (5,266,793) and Rostoker (5,339,262).**

*Regarding Claim 1*, Darty discloses:

An electrical power distribution center comprising:

a gateway module including logic to interface to a vehicle management computer (VMC) via a standard data bus (Figure 1, Item 10; Column 6, Lines 46-51), wherein the gateway module comprises redundant microcontrollers (Figure 3, Items 1 and 1'; Column 8, Lines 53-56) operably connected to the VMC (Figure 1, Item 10) for selectively controlling supply of electrical power to a plurality of separate electrical loads;

an internal serial data bus (Figure 1, Item 3), wherein the microcontroller is operably connected to the internal serial data bus (Column 6, Lines 5-7);

and a plurality of Load Management Modules (LMMs) (Figure 1, Items 5, 7, 9 and 11), each Load Management Module operably connected to the internal serial data bus for receiving control commands from the gateway module (Column 6, Lines 24-30), wherein each Load Management Module comprises:

a local microcontroller (Figure 5, Item 11a);

a plurality of power switching devices (Figure 5, Items 68-71); and

a plurality of discrete components corresponding to the plurality of power switching devices for interfacing the power switching devices to the local microcontroller (Figure 5, Items 54-57 and 64-67).

Darty does not disclose:

A dual redundant standard data bus for connecting the gateway module to the VMC;

Two internal serial data buses of different types, wherein the Load Management Modules and redundant microprocessors are each operably connected to the two internal serial data buses;

Each Load Management Module comprising a plurality of application specific integrated circuits.

Regarding the application specific integrated circuits, Maher teaches:

A solid state circuit controller (Figure 1) for switching power to a load and for protecting either the load or the wire (Column 1, Lines 8-11) comprising two integrated circuits referred to as Supply ASIC 12 and Control ASIC 14 (Figures 2 and 3; Column 4, Lines 57-59).

Rostoker teaches:

"Using one or more ASICs specially designed for an application, a system designer can dramatically reduce the number of components (integrated circuit devices and other electronic parts required to build and electronic system" (Column 1, Lines 36-40).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to replace the discrete components used by Darty to control the power switching devices in the Load Management Modules with the ASIC enabled power switching device described by Maher as a design choice for the well-known benefits described by Rostoker.

Regarding the dual redundant standard data bus connecting the gateway module to the VMC as well as the two internal serial data buses of different types, Smith teaches:

The use of "two microprocessors operating on different instruction sets to increase reliability with diverse redundancy" (Column 4, Lines 30-31).

The purpose of this redundancy is to "account for potential failure of system components" (Column 4, Lines 27-28). Although Smith does not specifically discuss the use of dual busses, his teachings underscore the concept of diverse redundancy. By incorporating different processors, a fault that would affect one processor will not necessarily affect the other processor, thereby increasing reliability.

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of the invention to design the power distribution control center demonstrated by the teachings of Darty and Maher with the teachings of redundancy and particularly diverse redundancy made by Smith in mind such that the communication lines between the gateway module and both the vehicle management controller and the load management modules. Smith's teachings show that in the case of the VMC, the homogeneous redundancy would provide increased communication reliability. Further, in the case of the internal serial data buses, the differing bus types would provide a strong degree of reliability as they provide diverse redundancy.

*Regarding Claim 15*, Darty further teaches:

at least one relay LMM (Figure 10; Column 20, Lines 50-53) having a plurality of relay devices (Column 10, Lines 53-57).

**3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and in further in view of Lee (6,735,709).**

*Regarding Claim 2*, Lee teaches:

A memory device with logic for internal reset and calibration sequences during a power-up initiation cycle (Column 2, Lines 5-6; Claim 27).

Lee provides motivation for his method, "system timing and output signal drive level calibration at start-up or reset is a very important aspect of the operation of such devices to compensate for wide variations in individual device parameters or within the system design itself" (Column 1, Lines 28-32). Lee further is interested in ensuring that "incoming data is correctly sampled and outgoing data is correctly timed" (Column 1, Lines 37-38).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to use the reset and calibration and method taught by Lee on ASICs used in a power distribution center during start up as taught by Darty, Maher, Rostoker and Smith so that the data transfers made between the claimed gateway module and the many load management modules associated with it may communicate without fear of error.

**4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Jouper (5,754,445).**

each ASIC is configurable for both AC and DC loads at a plurality of current ratings (Figure 2, Item 60; Column 7, Lines 5-8 and 15-18).

Jouper is motivated to include this feature so as to ensure the "power [is converted] into a form usable by electronic device 32a" (Column 6, Lines 66-67).

Accordingly, it would have been obvious to a person of ordinary skill in the art to provide the load management modules in a power distribution center as taught by Darty, Maher, Smith and Rostoker to be configurable to handle a variety of AC and DC inputs as taught by Jouper so

that the devices that the load management modules server will be able to handle the power accordingly.

**5. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Jones (4,811,136 and 4,782,422).**

*Regarding Claims 4-6*, Jones teaches:

each ASIC includes an analog processor (4,782,422; Figure 4, Item U2) that uses the $I^2t$ value to control variable trip times (4,811,136; Figure 3, Item 98) under different application configurations (4,782,422; Column 14, Lines 20-25).

Further, the production of a true RMS current value and the use of said RMS value for the calculation of an $I^2t$ value are considered inherent to the calculation of the $I^2t$ value detected by Jones.

Jones notes a use for this detection circuit would include a protective means for a circuit for when the $I^2t$ value exceeds a predetermined amount (Column 2, Lines 52-58).

Accordingly, it would have been obvious to a person of ordinary skill in the art to combine the teachings of a power distribution center provided by Darty, Maher, Smith and Rostoker with the use of a $I^2t$ tripping mechanism as taught by Jones for the purpose of protecting a circuit from an unacceptable large $I^2t$ value.

**6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Jaskolski (4,050,083).**

*Regarding Claim 7*, Jaskolski teaches:

each ASIC includes a thermal shut-down circuit (Figure 1, Item 7) that opens the corresponding power switching device (Figure 1, Item 4) when a substrate (Figure 1, Item 5) of the power switching device exceeds a predetermined reference temperature (Columns 6 and 7, Lines 65-68 and 1, respectively).

Jaskolski is motivated by the desire to "automatically . . . protect the power switch against overheating" (Column 3, Lines 47-49)

Accordingly, it would have been obvious to a person of ordinary skill in the art to use a thermal shutdown circuit as taught by Jaskolski in the system of power distribution control as taught by Darty, Maher, Smith and Rostoker so as to provide further protection of the components within the system.

*Regarding Claim 8*, Jaskolski further teaches:

the predetermined reference temperature is adjusted using an external setting resistor (Figure 2, Item 20; Column 7, Lines 7-9).

**7. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Jones (4,811,136).**

*Regarding Claims 9 and 11*, Jones teaches:

each ASIC includes logic for zero-crossing current detection (Figure 3, Item 88)and zero-crossing voltage detection (Figure 3, Item 74).

Jones provides motivation for these detections of these faults so that problems in the power source may be detected and corresponding loads may be switched to a new power source with minimal supply interruption (Column 2, Lines 34-41).

Accordingly, it would have been obvious to a person of ordinary skill in the art to use the power supply fault detecting means taught by Jones with the power distribution center taught by Darty, Maher, Smith and Rostoker so that the power supplied to the many loads in the distribution center can suffer minimal interruption in power availability.

*Regarding Claim 10*, Jones further teaches:

the zero-crossing current detection and zero-crossing voltage detection are used for controlling off/on activation timing of the corresponding power switching device when operating in an AC mode (Column 7, Lines 33-42).

**8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Levran (5,982,645).**

*Regarding Claim 12*, Levran teaches

each ASIC includes logic for a soft-start function (Figure 4i, Item 350) when operating in a DC mode (Column 22, Lines 65-67).

Levran teaches motivation by saying "A soft start signal is desired when the AC to DC power conversion system is first activated in order to prevent excessive inrush current or other clamping which may occur during normal operation of the power conversion system" (Column 22, Lines 59-64).

Accordingly, it would have been obvious to a person of ordinary skill in the art to provide the soft start feature taught by Levran into the ASICs taught by Darty, Maher, Smith and Rostoker for the purposes of providing the circuits with a protective element associated with the startup phase in the power distribution center.

**9. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Daum (6,242,922) and David (5,604,385).**

*Regarding Claims 13 and 14*, David teaches:

Current sensors 16, 18, 20 [to] measure the current flowing through phases $\phi 1$, $\phi 2$ and $\phi 3$, respectively (Column 2, Lines 37-38).

An array of multi-pole switches 22, 24, 26, 28, 30 (Column 2, Lines 44-45).

David provides as motivation for his control method the need to "evenly distribute electrical power across from the three incoming phases, supplied by the electric utility, to all branch circuits (Column 1, Lines 25-27).

David does not teach the gang operation of ASICs to implement his control method of a three phase power source.

However, Daum teaches:

An ASIC (Figure 1, Item 10) that implements a current sensor (Figure 1, Item 14; Column 4, Lines 15-17).

Daum provides motivation for this, teaching the "fabrication cost of the ASIC can be substantially less than the fabrication cost associated with known arc detection units" (Column 2, Lines 4-6).

Accordingly, it would have been obvious to use the ASIC-implemented current sensors taught by Daum for each of the three current sensors used in the method for controlling a three phase power distribution network as taught by David for the purpose of reducing fabrication costs of the device. Further, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a three phase power distribution network as taught by Daum into the power distribution center taught by Maher, Smith and Rostoker for the purpose of providing even distribution of electrical power throughout the electrical system.

**10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Miesterfeld (4,742,349).**

*Regarding Claim 16*, Miesterfeld teaches:

the serial data buses being in either a Synchronous Serial Peripheral Interface mode of data transfer (SPI) (Column 4, Lines 8-10) or an Asynchronous Serial Communications Interface (SCI) mode (Column 4, Lines 3-4).

Miesterfeld further teaches the implementations of the two modes of data transfer require different hardware (Figures 1 and 2).

Accordingly, it would have been obvious to a person of ordinary skill in the art to combine the teachings of these two specific forms of serial communication that are similar in function, but different in form as shown by Miesterfeld with the teachings of diversely redundant

busses as taught by Darty, Maher, Smith and Rostoker for the purposes of providing this diverse redundancy.

**11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Matsumaru (5,818,673).**

*Regarding Claim 17*, Matsumaru teaches:

each power switching device (Figure 6, Item 7) comprises a fusible link (Figure 6, Item 15) to cause an open circuit in case of a short circuit failure of the power switching device (Column 3, Lines 12-20).

Matsumaru provides motivation by stating "supply of electric power to the downstream position, at which the short circuit has taken place, is interrupted so that a secondary disaster, such as a fire, is prevented" (Column 3, Lines 20-23).

Accordingly, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Maher, Smith and Rostoker with the teachings of Matsumaru so that catastrophic problems in the power switching devices contained in the power distribution system may be prevented.

**12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith, Rostoker and Matsumaru in further view of Thomas (6,331,763).**

*Regarding Claim 18*, Thomas teaches:

the fusible link is a MOSFET (Figure 39, Item 232) wirebond (Figure 39, Item 230).

Thomas is motivated by the desire to provide protection to the circuit in the event of a MOSFET failure (Column 21, Lines 48-49).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention, for the purposes of preventing damage due to short circuit, to implement a MOSFET wirebond as described by Thomas in the fusible link described by Matsumaru.

**13. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith and Rostoker and further in view of Schmidt (5,550,702).**

*Regarding Claim 19*,

each power switching device (Figure 5; Column 4, Lines 27-32) comprises:

a thermal sensor (Figure 5, Item $T_{s1}$);

a sense resistor (Figure 5, Item $R_1$);

and a plurality of MOSFETs (Figure 5, Items $M_1$; $FF_1$ and $FF_2$ also contain MOSFET transistors).

Schmidt presents the desire for "protecting power devices on an integrated circuit from destructive overloads" (Column 4, Lines 10-11).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to combine the teachings of the protective method described by Schmidt with the teachings of the power distribution center described by Darty, Maher, Smith and Rostoker for the purposes of providing the power distribution center protection from dangerous overloads of the circuitry in the system.

**14. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, Maher, Smith, Rostoker, Schmidt and further in view of Matsumaru (5,818,673) and Thomas (6,331,763).**

*Regarding Claim 20*, Matsumaru teaches:

a fusible link (Figure 6, Item 15) to cause an open circuit in case of a short circuit failure (Column 3, Lines 12-20) of the power switching device (Figure 6, Item 7).

Matsumaru does not teach:

each MOSFET includes a fusible link, wherein the fusible link is a MOSFET wirebond.

Thomas teaches:

each MOSFET (Figure 39, Item 232) includes a fusible link, wherein the fusible link is a MOSFET wirebond (Figure 39, Item 230).

The motivations for combining Matsumaru and Thomas with the teachings of Darty, Maher, Smith, Rostoker and Schmidt can be seen, respectively, in the above Claim 17 and 18 rejections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAH

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